

SEMESTER S6

SEMICONDUCTOR DEVICE MODELING

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|--|--------------------------------|--------------------|----------------|
| Course Code | PEEVT 636 | CIE Marks | 40 |
| Teaching Hours/Week (L: T:P: R) | 3-0-0-0 | ESE Marks | 60 |
| Credits | 3 | Exam Hours | 2 Hrs. 30 Min. |
| Prerequisites (if any) | Solid State Devices (PCECT302) | Course Type | Elective |

Course Objectives:

1. This course explains the qualitative understanding of the physics of the semiconductor devices and conversion of this understanding into equations
2. To introduce students to the field of compact modeling and familiarize them with the methods for the model development

SYLLABUS

| Module No. | Syllabus Description | Contact Hours |
|-------------------|---|----------------------|
| 1 | Semiconductor device modeling overview: Types of device models- Numerical Models, Analytical models, compact models. PN Junction diode: DC Current-Voltage Characteristics, Limitations of the ideal diode model, Static model of the ideal diode and its implementation in SPICE2, Static model of the real diode and its implementation in SPICE2, Large-signal model of the diode, Small-signal model of the diode, Temperature and area effects on the diode model parameters. | 9 |
| 2 | Bipolar junction transistor : Ebers-Moll static model, Ebers-Moll large signal mode , Ebers-Moll small signal model, Gummel – Poon static model, Temperature and area effects on the BJT model parameters. Heterojunction Bipolar junction transistor (HBT): SiGe HBT, Static operation and characteristics, HICUM level 2: Internal transistor model. | 9 |
| 3 | The four terminal MOS structure: strong inversion, complete symmetric strong inversion model, simplified symmetric strong inversion model, simplified source referenced strong inversion model. MOS Transistor SPICE models: Level 1 static model, level 2 static model, | 9 |

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|----------|---|----------|
| | level 1 and level 2 large signal model, small signal model, effect of temperature on the model parameters. MOSFET BSIM models: BSIM1 model, parameter listing, BSIM1 static model, BSIM1 charge model. | |
| 4 | MOSFET BSIM models: BSIM1 model, parameter listing, BSIM1 static model, BSIM1 charge model. Advanced semiconductor device modeling: Tunnel FET: need of TFET, device structure, TFET modelling approach, modelling the surface potential source channel junction: pseudo 2D method, modelling drain current: constant polynomial term assumption, tangent line approximation. Modeling of novel unipolar devices: Device structures and principles of operation of FinFET, HEMT, TFET. Basic modeling concepts- | 9 |

Course Assessment Method
(CIE: 40 marks , ESE: 60 marks)

Continuous Internal Evaluation Marks (CIE):

| Attendance | Assignment/ Microproject | Internal Examination-1 (Written) | Internal Examination- 2 (Written) | Total |
|-------------------|-------------------------------------|---|---|--------------|
| 5 | 15 | 10 | 10 | 40 |

End Semester Examination Marks (ESE)

In Part A, all questions need to be answered and in Part B, each student can choose any one full question out of two questions

| Part A | Part B | Total |
|---|--|--------------|
| <ul style="list-style-type: none"> ● 2 Questions from each module. ● Total of 8 Questions, each carrying 3 marks <p style="text-align: center;">(8x3 =24marks)</p> | <ul style="list-style-type: none"> ● Each question carries 9 marks. ● Two questions will be given from each module, out of which 1 question should be answered. ● Each question can have a maximum of 3 sub divisions. <p style="text-align: center;">(4x9 = 36 marks)</p> | 60 |

Course Outcomes (COs)

At the end of the course students should be able to:

| Course Outcome | | Bloom's Knowledge Level (KL) |
|----------------|---|------------------------------|
| CO1 | Implement the static model of an ideal diode and a real diode in SPICE2 software, demonstrating the ability to set up and run simulations. | K3 |
| CO2 | Implement and simulate the Ebers-Moll and Gummel-Poon static models for BJTs in SPICE2, demonstrating practical application skills. | K3 |
| CO3 | Explain the differences between the complete symmetric strong inversion model, the simplified symmetric strong inversion model, and the simplified source-referenced strong inversion model for MOS structures. | K2 |
| CO4 | Explain the TFET modeling approach and the importance of modeling the surface potential at the source-channel junction. | K2 |

Note: K1- Remember, K2- Understand, K3- Apply, K4- Analyse, K5- Evaluate, K6- Create

CO-PO Mapping Table:

| | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|
| CO1 | 3 | 2 | 2 | | 1 | | | | | | | |
| CO2 | 3 | 2 | 2 | | 1 | | | | | | | |
| CO3 | 3 | 2 | 2 | | 1 | | | | | | | |
| CO4 | 3 | 2 | 2 | | | | | | | | | |

| Text Books | | | | |
|------------|---|-------------------------|-------------------------|------------------|
| Sl. No | Title of the Book | Name of the Author/s | Name of the Publisher | Edition and Year |
| 1 | COMPACT HIERARCHICAL BIPOLAR TRANSISTOR MODELING WITH HICUM | Michael Schroter | World Scientific | 1/e, 2010 |
| 2 | Semiconductor Device Modeling With SPICE | Giuseppe Massobrio | McGraw-Hill | 2/e, 1993 |
| 3 | Tunnel Field-Effect Transistors (TFET) Modelling and Simulation | Jagadesh Kumar Mamidala | John Wiley | 1/e, 2017 |
| 4 | Operation and Modelling of the MOS Transistor | Yannis Tsididis | Oxford University Press | 3/e, 2010 |

| Reference Books | | | | |
|------------------------|--|-----------------------------|------------------------------|-------------------------|
| Sl. No | Title of the Book | Name of the Author/s | Name of the Publisher | Edition and Year |
| 1 | SEMICONDUCTOR DEVICES MODELLING AND TECHNOLOGY | Nandita Das Gupta | PHI learning | 1e/2004 |
| 2 | Semiconductor Device Modelling | Christopher M. Snowden | Springer | 1e/2012 |
| 3 | Semiconductors Physics and Devices | Donald Neamen | Tata Mc Graw Hill | 4e/2017 |
| 4 | Physics of Semiconductor Devices | S M Sze | Wiley | 3e/2007 |

| Video Links (NPTEL, SWAYAM...) | |
|---------------------------------------|---|
| Module No. | Link ID |
| 1 | https://nptel.ac.in/courses/117106033 |
| 2 | https://nptel.ac.in/courses/117106033 |
| 3 | https://nptel.ac.in/courses/117106033 |
| 4 | https://www.youtube.com/playlist?list=PLbMVogVj5nJQ2k2HAGHFENB4a2nI8OppN |